Improved Transfer of Graphene for Gated Schottky-Junction, Vertical, Organic, Field-Effect Transistors

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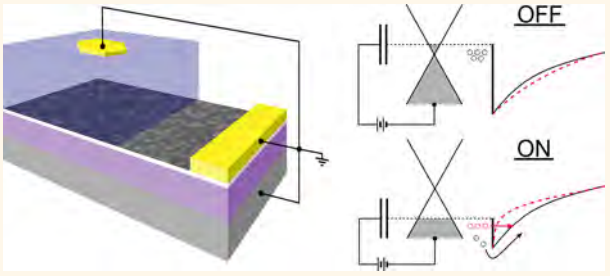
ABSTRACT



An improved process for graphene transfer was used to demonstrate high performance graphene enabled vertical organic field effect transistors (G-VFETs). The process reduces disorder and eliminates the polymeric residue that typically plagues transferred films. The method also allows for purposely creating pores in the graphene of a controlled areal density. Transconductance observed in G-VFETs fabricated with a continuous (pore-free) graphene source electrode is attributed to modulation of the contact barrier height between the graphene and organic semiconductor due to a gate field induced Fermi level shift in the low density of electronic-states graphene electrode. Pores introduced in the graphene source electrode are shown to boost the G-VFET performance, which scales with the areal pore density taking advantage of both barrier height lowering and tunnel barrier thinning. Devices with areal pore densities of 20% exhibit on/off ratios and output current densities exceeding 10^6 and 200 mA/cm^2, respectively, at drain voltages below 5 V.

KEYWORDS: graphene · transparent electrode · vertical field effect transistor · organic transistors

To first approximation the work function difference between a metal and a semiconductor dictates the transport across their junction, determining whether the contact will be Ohmic or have a Schottky barrier to electrical transport.[1,2] Conventional metals possess a large density of electronic states (DOS), requiring the addition/subtraction of large amounts of charge to induce appreciable shifts in their work functions (like the water level in a large lake, much water must be added to change the level perceptibly). This picture changes dramatically for low DOS metals like carbon nanotubes and graphene for which charge addition/subtraction induces much more dramatic work function, or equivalently, Fermi level shifts (for a tall narrow glass, little water is needed to change the level appreciably). Since the Fermi level in these materials can be changed in response to gating fields, these low DOS carbon-based metals, placed in contact with a semiconductor, admit a new mechanism for current modulation by the gate field control of their trans-junction transport. That is, by tuning of the Schottky barrier height. This allows for new high performance device architectures.

Such control has been demonstrated in the carbon nanotube enabled vertical field effect transistor (CN-VFET) where modulation of the contact barrier between a dilute nanotube source electrode and an organic semiconductor channel layer controls the current flow through the organic channel.[3−5] This vertical architecture—consisting of a gate, gate dielectric, source electrode, semiconducting channel, and drain electrode in a collinear stack (similar to Figure 1a here)—took advantage of the very thin control layer occurring at the nanotube−organic junction, allowing for short channel lengths and yielding high on-currents at low source−drain voltage. The architecture, moreover, readily lent itself to conversion to a full aperture emission light emitting transistor, which operated at high brightness with a low power dissipation.[6]

The increasing availability of high quality graphene[7−10] and the low DOS it shares with the nanotubes makes graphene a natural candidate source electrode for similar high performance VFETs. This architecture, vertically stacking the source, channel, and

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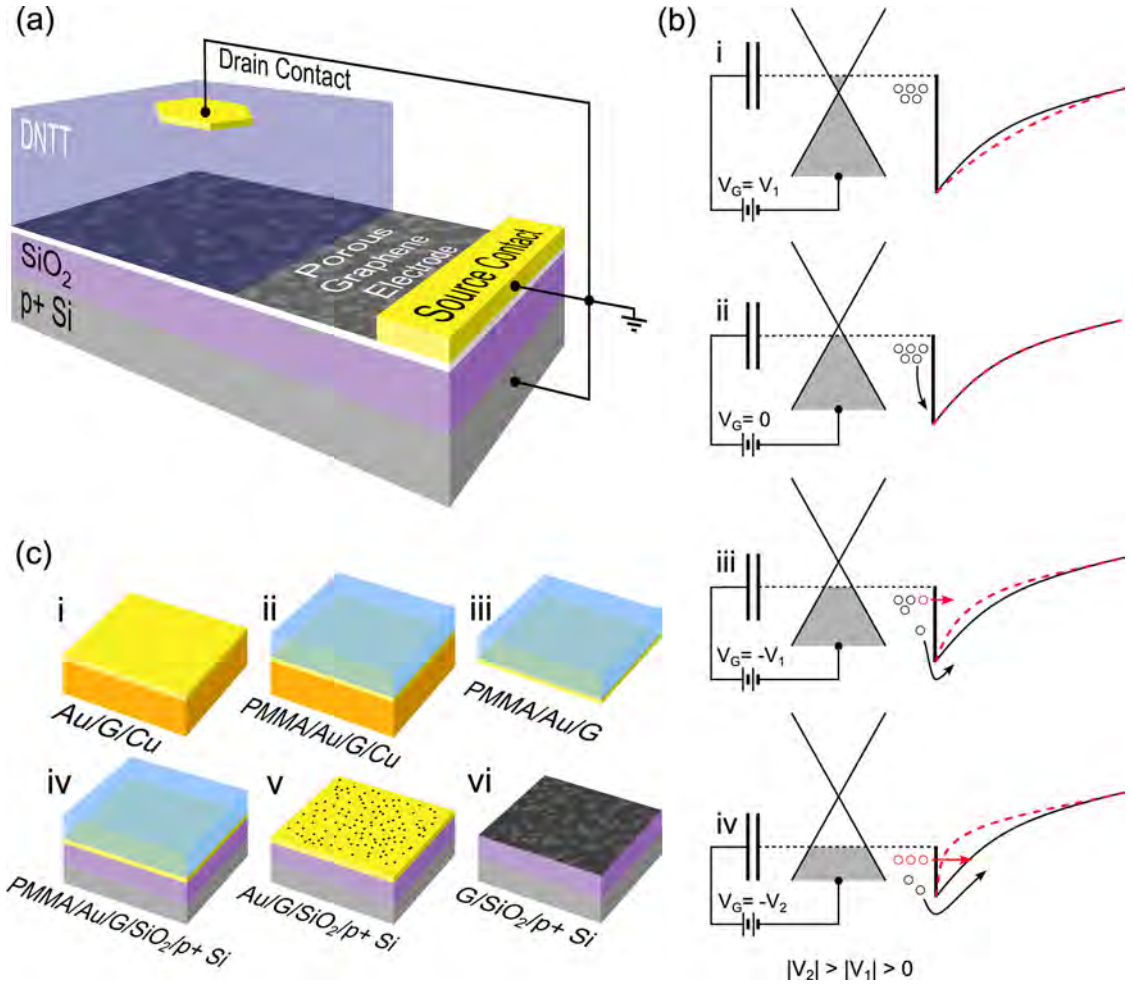

Figure 1. (a) G-VFET architecture and drive scheme. (b) Energy level diagram for a G-VFET at the graphene-semiconducting channel interface for constant drain voltage and three distinct gate voltages. The black line depicts the hole injection barrier and depletion layer in the semiconductor for a continuous graphene electrode. The red dashed line depicts the same features for the case of a graphene electrode perforated with holes (as discussed below). For the continuous graphene case current modulation is due principally to barrier height lowering (thermionic emission). For the perforated graphene case the barrier also thins (enhancing tunneling): (i) a negative gate bias shifts the graphene work function increasing the barrier for hole injection into the organic; (ii) the Schottky barrier and band bending induced by the offset of the intrinsic graphene work function (slightly p-type) with the HOMO level of the organic semiconductor; (iii) moderate positive gate bias shifts the graphene work function in a direction that decreases the barrier height. The band bending is more pronounced for the perforated graphene; (iv) at high gate bias the barrier height is significantly reduced and the depletion width dramatically thinned for the case of perforated graphene. (c) Schematic of the graphene source electrode fabrication process using a protective evaporated Au layer: (i) the Au film evaporated onto the as-grown graphene on Cu, (ii) PMMA spin coated onto the gold layer, (iii) Cu etched away, (iv) graphene/Au/PMMA stack adhered to the dielectric layer on p^+Si, (v) PMMA etched away in O_2 plasma (spots depict pinholes in the Au film), (vi) Au film etched away leaving behind a residue-free, perforated graphene sheet.

drain layers (Figure 1a), makes the transistor channel length simply the thickness of the deposited channel layer. Short channel lengths permit large on-currents, despite the use of relatively low mobility organic semiconductors. For a conventional, lateral channel, TFT to achieve a comparable channel length would require (expensive) high resolution patterning.

The monolithic nature of graphene may provide intrinsic advantages in sheet resistance compared to nanotube films, where impedance at tube−tube junctions may ultimately limit device performance.[11,12] The single atom thickness of graphene in a continuous layer also affords the opportunity to disentangle the operational mechanism of these gated Schottky junction VFETs. Above we highlighted the barrier *height* modulation made available by the low DOS nanotubes, but VFETs that use conventional metal source electrodes (in which the high DOS effectively precludes such barrier height modulation) have also been demonstrated.[13−16] To function those devices require that the metallic source electrode be perforated, thus allowing the gate field direct access to the metal−semiconductor interface, where a field−induced band bending *thins* the barrier (without the Fermi level shift induced barrier height lowering) to allow tunneling currents. Such band bending also contributes to barrier modulation in the CN-VFET, where the dilute nanotube source electrode also admits the gate field to

the nanotube−organic interface. The nanotube-based devices thus operate in a mixed fashion, taking advantage of both modes. The *continuous* electrode provided by graphene can probe (principally) the effect of the barrier height modulation. Better still, by purposely creating holes in the continuous graphene layer we can probe both modes in a single material system (Figure 1b). Here this is done to report the first organic channel graphene enabled VFETs (G-VFETs).

RESULTS AND DISCUSSION

In the G-VFET device architecture (Figure 1a) the thin channel layer between the graphene source and top drain electrodes imposes rather severe requirements on the quality of the graphene layer, at least in terms of minimizing vertical protrusions. The conventional polymethylmethacrylate (PMMA) transfer method[7] for copper-based chemical vapor deposition (CVD) grown graphene was found to be unreliable, with numerous tears and wrinkles causing frequent shorting pathways to the top drain electrode. Techniques described in the literature to improve the PMMA transfer were tried;[17,18] however, these did not fully eliminate damage induced by the swelling of the PMMA during acetone dissolution. A modified PMMA transfer method was developed that gave much better results. Transfer of CVD grown graphene from the copper growth substrate was improved by depositing a thin layer ($\leq$100 nm) of Au as a protective layer before spinning the PMMA support film ensuring a post-transfer surface that is free of difficult to remove polymeric residue. The thin metallic layer avoids strain induced by the swelling of the PMMA film during the more conventional transfer process. This is especially important at domain boundaries where chemical bonding between the polymeric chains and the graphene is favorable.[19]

Figure 1c illustrates the procedure for transferring and patterning the graphene using an Au thin-film as a protective layer and etch mask. Gold was thermally evaporated at a thickness ranging from 20 to 100 nm through a rectangular shadow mask onto graphene grown on polished copper foils, followed by spin coating the PMMA (further details in Methods and Supporting Information). After copper dissolution, the Au coated section of the graphene/Au/PMMA sandwich was adhered, graphene side down, to a p^+Si/SiO_2/BCB substrate. BCB is a benzocyclobutene derivative that had previously been spun coat onto the SiO_2 and thermally cross-linked to leave an 8 nm thick hydrophobic layer on the dielectric (thin BCB layer not indicated in Figure 1c). This excludes water adsorption from the ambient which has been implicated in charge trap generation on oxide dielectrics, degrading device performance.[20] The Au served as an etch mask while the PMMA and excess graphene around the gold mask were dry-etched in an O_2-plasma thus defining the edge of the graphene source electrode. An iodide based gold etchant subsequently removed the mask layer. Finally, a gold source contact was evaporated along one edge of the graphene layer completing the source electrode.

Micrometer scale holes with a crudely controlled density were produced in the graphene by varying the thickness of the Au mask layer. Thin Au layers possess submicrometer pinholes, with a through-hole density that depends on the layer thickness. During the dry etch of the PMMA, reactive oxygen radicals penetrate these holes to etch the graphene and underlying BCB, leaving behind circular holes in the graphene with an average diameter of 2−3 μm. The diameters of these holes are self-limiting due to the increasing diffusion path length for counter-propagating oxygen and reaction products in the confined space between the Au and the SiO_2, as the etched region grows. The measured areal hole densities in the graphene used to build the G-VFETs discussed below were 0, 2, 13, and 20% with average hole diameters of 2.2 $\pm$ 0.6 μm, 2.3 $\pm$ 0.6 μm, and 2.5 $\pm$ 1.0 μm, respectively.

Figure 2 compares the quality of the graphene transferred with and without the use of a thicker ($\sim$100 nm, pinhole-free) protective Au layer. Raman spectroscopy provides a comparative measure of graphitic materials, capable of distinguishing single-layer graphene from multilayer graphene and graphite,[21] and characterizing disorder, crystalline grain size, stacking symmetry, and doping of the graphene films.[22−24] The D to G-band intensity ratios are shown *versus* the full width at half maximum (fwhm) of the 2D-band overtone for 100 distinct points for the graphene films transferred with and without the use of the gold protective layer. The D-band was below the noise threshold (standard deviation of 50 counts *versus* a mean G-band peak height of 500 counts), and the 2D-fwhm was substantially reduced in the majority of measured spots for the Au protected films. Scanning electron (SEM) and atomic force micrographs (AFM) of films transferred by the two methods are shown in Figure 2 panels b and c, respectively. The films transferred using the gold protective layer are continuous, without the polymer residue, microtears, and wrinkles characteristic of the standard PMMA transfer.

The organic semiconductor channel layer evaporated onto the graphene was dinaphtho-[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT).[25] The flatness of a single layer of graphene should in principle permit even sub-100 nm channel layer thickness (with corresponding performance enhancement) without incurring electrical shorts to the top drain electrode. We found however that device yields suffered when the DNTT thickness was below 250 nm. This is likely a consequence of the low surface energy of graphene and the crystallinity of DNTT that results in island

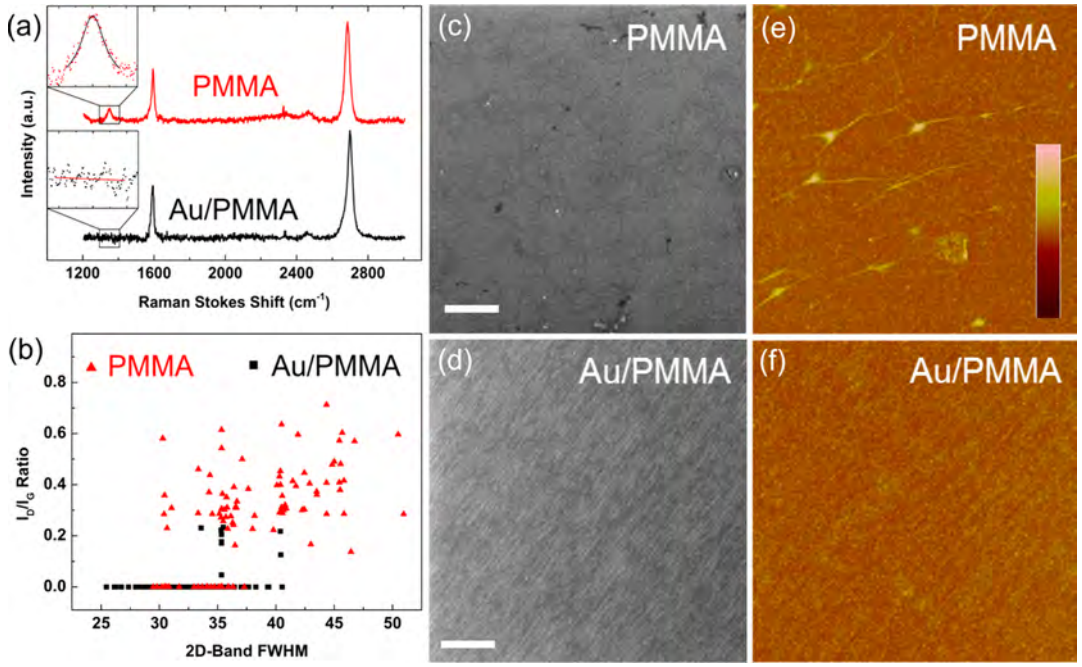

Figure 2. (a) Representative Raman spectra of the PMMA and Au/PMMA transferred graphene on BCB/SiO_2. Insets are zoomed in on the D-band regions. (b) Raman spectral data in the form of a cluster plot of D/G peak ratios *versus* the 2D-band FWHMs for a graphene layer transferred using the Au protected process (black squares) and a graphene layer transferred using the conventional PMMA process (red triangles). One hundred points were recorded on each layer in a square array having a pitch of approximately 50 μm. A smaller D/G ratio and fwhm are desirable, as seen for the majority of points recorded for the Au-transferred layer. (c, d) SEM (scale bars, 2 μm) and (e, f) AFM images (15 $\times$ 15 μm) of graphene layers transferred to SiO_2 using the Au-protected and the conventional PMMA processes, as indicated by the labels (75 μm height scale).

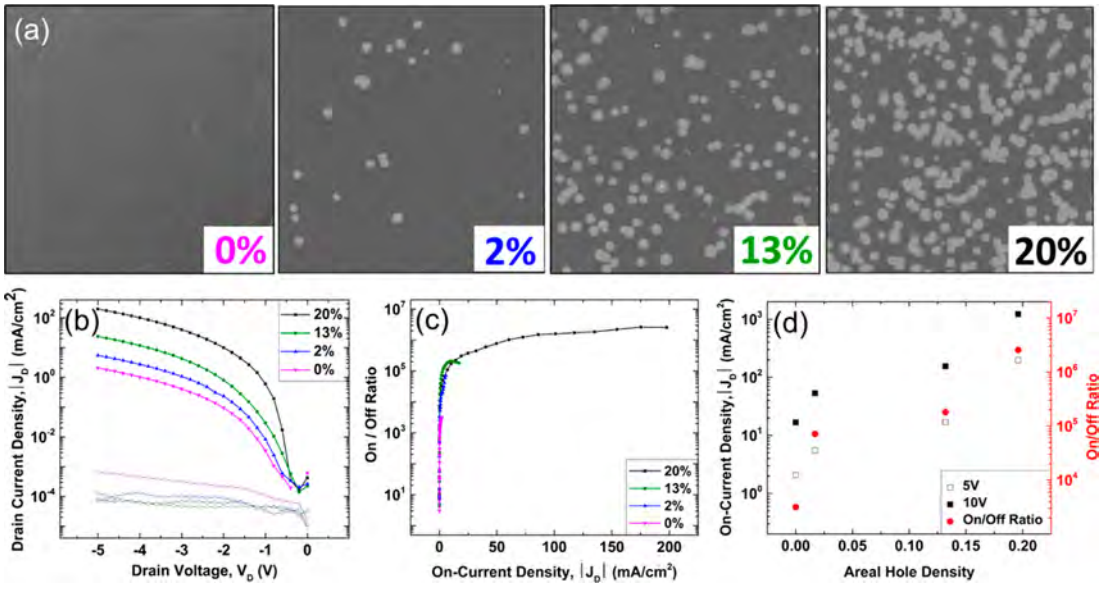

Figure 3. (a) SEM images (50 μm $\times$ 50 μm) of the transferred graphene films having the indicated hole densities. (b) G-VFET output curves for the off-state (V_G = +40 V, open symbols) and the on-state (V_G = −40 V, filled symbols) for these graphene source electrode hole densities. (c) On/off current ratio *versus* on-state current density up to a drain voltage of −5 V for each hole density. (d) On-current densities and on/off current ratios for drain voltage up to 10 V *versus* source electrode hole density.

growth incorporating pinholes and shorting paths to the subsequently deposited Au drain electrode in the case of thin channel layers. To ensure effectively 100% yields and to permit a direct performance comparison against comparable channel thickness CN-VFETs, a DNTT channel thickness of 500 nm was used.

G-VFET devices were tested with the graphene source electrode contact held at ground potential, while the drain and gate were biased relative to ground. Figure 3b shows typical output curves for the G-VFETs with graphene source electrode areal hole densities of 0, 2, 13, and 20% (Figure 3a). Both the on

(V_G = −40 V) and off (V_G = +40 V) states are shown. Thinner and/or higher-*k* gate dielectrics should allow for low gate voltage operation as seen in CN-VFETs that employ them.[4,6] The advantage of the short channel length in the vertical architecture is seen in the high on-current densities at low drain voltages (≤|−5| V). The on-current densities clearly scale with the density of holes in the graphene source electrode. Figure 3c plots the on/off current ratio of the devices as a function of the on-current density (as the drain voltages are swept from 0 to −5 V). The 20% areal hole density electrode device yields on/off ratios exceeding 10^6. Attempts to get higher hole densities (>20%) by making the protective Au layer thinner resulted in discontinuous graphene sheets. Ordered hole arrays would avoid this problem and provide a path for further device optimization. A summary of the device characteristics *versus* areal hole density is plotted in Figure 3d.

The current modulation seen to occur with the continuous graphene electrode (over 3 orders of magnitude) provides strong support for the anticipated Schottky barrier height modulation (changing principally the thermionic emission). Extrapolating from the Kelvin probe measurements of Yu *et al.*,[26] we estimate that our gate sweep results in a 0.4−0.5 eV shift of the graphene work function and a commensurate modulation of the barrier height. Introducing 20% holes into the graphene source electrode yields a further 2−3 decades of transconductance. The gate field access to the graphene−DNTT interface in the vicinity of the holes additionally thins the barrier (Figure 1c) resulting in the dramatic current enhancement. Note that barrier height modulation also plays a role in the enhanced tunneling currents since (for example) within the WKB approximation the tunneling probability is proportional to $\exp[-k\phi_{bh}^{3/2}/E]$ where ϕ_{bh} is the barrier height, E the local electric field, and k is constant. Such barrier height modulation can thus explain the dramatic performance advantage these low DOS metals (graphene, nanotubes) have over the conventional-metal source electrode based devices. Our work expands on recent studies of the (ungated) transport across nanotube/organic-semiconductor[27,28] and graphene/inorganic-semiconductor junctions.[29]

A comparison between the G-VFET and CN-VFET reveals differences that can be attributed to the morphological differences between the respective source electrodes. Figure 4a compares transfer curves for a G-VFET with a 20% areal hole density graphene source electrode and a typical CN-VFET fabricated on identical p^+Si/SiO_2/BCB substrates. The drain voltages are adjusted to yield comparable on-currents at a gate voltage of −40 V. The large hysteresis seen in the nanotube-based device has been explained by ambipolar charge traps in the BCB having a well-defined critical field for charge exchange with the electrode.[30] This hysteresis can be minimized by restricting the gate

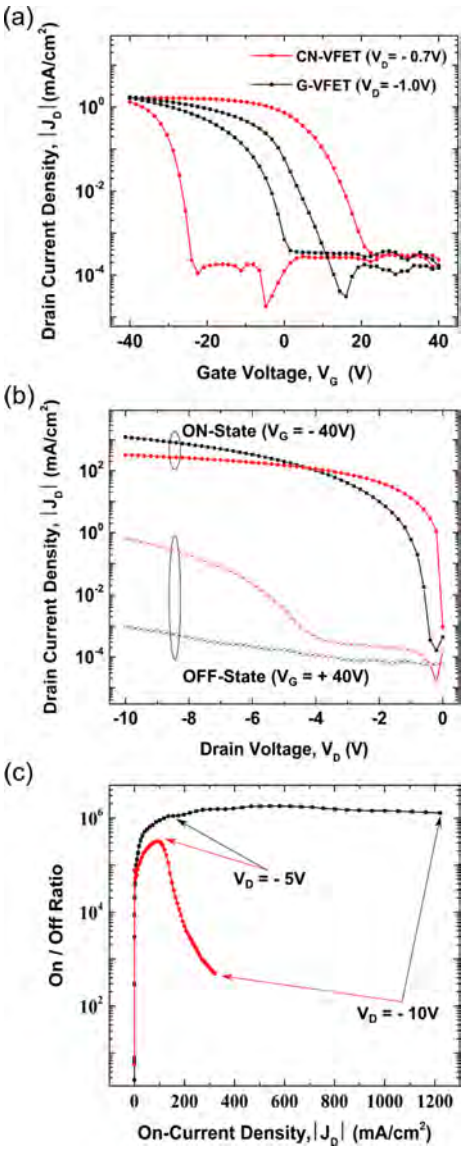

Figure 4. Comparison of graphene and carbon nanotube enabled VFETs with all other device layers the same. (a) Transfer curves for a CN-VFET and the G-VFET with a 20% areal hole density electrode. (b) Output curves for both devices in the on (V_G = −40 V) and off (V_G = +40 V) states up to V_D = −10 V. (c) On/off ratios *versus* on-current density for drain voltages to −10 V.

voltage range but here it is interesting to observe the significantly smaller hysteresis for the graphene source electrode over the same large voltage range. Since the gate field provides the driving force for charge injection into the traps the larger gate field concentration around the line-like nanotubes, *versus* that for the half-plane like graphene near the edge of a hole, would (for the same applied voltage) drive more charge injection into traps around the nanotubes.

Output curves for the two devices are plotted in Figure 4b for gate voltages of ±40 V and drain voltages out to −10 V. Compared to the nanotube device the graphene devices exhibit a drain voltage delay of ∼500 mV before current begins to flow. This may

be due to the work function difference between the graphene (−4.6 eV) and the DNTT (−5.4 eV) generating a larger initial barrier than that between the DNTT and the nanotubes. The nitric acid purification of the nanotubes charge transfer dopes them, placing their work function around −4.9 eV, after which a heating step dedopes them to an estimated −4.7 to −4.8 eV. The field concentration around the nanotubes may also give them an advantage in terms of this lower turn-on voltage. As the drain voltage continues to grow, the nanotube device off-current begins to suffer as the drain field concentration around the nanotubes begins to extract charge despite the off-state (+40 V) gate voltage. The planar graphene does not exhibit such degradation in the off-state. The graphene electrode also excels in the on-state at high drain voltage. At V_D = −10 V the CN-VFET on-current density is ∼300 mA/cm^2 compared to an astounding ∼1200 mA/cm^2 for the graphene device. We attribute this to the lower impedance of the monolithic graphene layer *versus* that at tube−tube contacts across the nanotube film electrode. Figure 4c compares the on/off ratios for the two devices as a function of their on-currents (V_G = −40 V) as the drain voltage is swept from 0 to −10 V. The impedance limited on-current and increasing off-current degrades the on/off ratio of the nanotubes device while that of the graphene device remains above 10^6 out to −10 V.

CONCLUSION

Better controlled patterning techniques to fabricate ordered hole arrays in graphene over a wider range of densities and sizes, in conjunction with a thinning of the active channel layer thickness should offer a straightforward path to improved device performance. Optimized nanotube devices yield their highest on/off ratios with an areal pore density of approximately 75% suggesting significant room for improvement in such organic channel graphene devices.

Our work here also has implications for a very recently published inorganic channel graphene source electrode FET labeled a "Barristor".[31] While that device used a top gate architecture and the semiconductor was crystalline silicon, the principle of operation can be recognized to be precisely the same as the *continuous* graphene bottom gate, organic semiconductor devices we discuss here (unlike the case for the relatively low mobility organic semiconductors, the high mobility of the crystalline silicon allows the drain electrode to lie in a more remote, arbitrary location relative to the graphene source electrode without loss of performance). Their (and our) Schottky junction devices exhibit a gate modulated transconductance in either the forward or reverse bias direction of the graphene/semiconductor diode. In the case of a continuous graphene source electrode, which relies principally on barrier height modulation, they show a forward bias on/off ratio of 10^5, which greatly exceeds the performance of transistors that use graphene as the channel layer. However, attaining the low off-state current in the forward direction of the diode required an impractically low bias voltage of 0.3 V (the off-state current rising much more quickly than the on-state current as the bias voltage increased, resulting in the rapid decay of the on/off ratio). In reverse bias operation their on−off current ratio was only a factor of 300, approaching the 3 orders of magnitude current modulation we show for the *continuous* graphene/organic semiconductor operating in reverse bias. As we further show, however, providing the gate field direct access to the graphene/semiconductor interface by incorporating holes or edges in the graphene electrode introduces a new tunneling mechanism that boosts the on/off ratio by an additional 3 orders of magnitude to yield a ratio of 10^6. By operating our field porous graphene/organic channel devices in the reverse bias mode the off-state was maintained even to large bias voltages (as expected for a diode operated in reverse bias), while the on-state was dramatically boosted by tunneling through the thinned Schottky barrier in those regions where the gate field now had direct access to the graphene/semiconductor interface. Similar large improvements should be had by configuring the graphene/silicon devices to allow such gate field access when operated in reverse bias.

These results demonstrate the tremendous potential of graphene as an effective source electrode for Shottky junction field effect transistors. Our modified transfer technique that facilitated the use of graphene in these devices should also find use in other applications.

METHODS

Copper foils (99.98% purity, oxygen-free Cu, American Elements) 50 μm thick were chemically mechanically polished (CMP) at Sinmat Inc. on a Buehler Ecomet-300/Automet-250 benchtop polisher using a Suba-IV pad (Eminess). The CMP slurry was prepared with 10 wt % colloidal silica (∼75 nm nominal particle size) in a 5 vol % H_2O_2 solution, using 25 mM benzotriazole as a corrosion inhibitor, and 100 mM citric acid as a complexing agent. The acidity of the slurry was adjusted to a pH of 5 using NH_4OH. Polishing was done with a down-pressure of 3 psi, the platen and head rotating at 90 and 60 rpm, respectively, and a slurry flow rate of 40 mL/min. Approximately 2−3 μm of copper was polished away to achieve a smooth surface. Foils were subsequently exposed to a dilute HF (250:1, DI:HF) solution to etch away residual slurry particulates and rinsed in pure DI water.

Li *et al.*[32] demonstrated increased grain size of single layer graphene on the inside of copper foil enclosures formed by rolling and crimping the foil. Rather than crimp our CMP

polished copper foil substrates, flat pieces were placed inside covered tantalum boats (R.D. Mathis Company, SB-4/SB-4A) which improved ease of handling and reproducibility. Tantalum was chosen based on the following merits: it has a high melting point and good mechanical stability; it is a good oxygen scavenger; it has a low sticking coefficient for Cu; it is inexpensive.

The tantalum enclosed foil samples were placed in a 1.5" diameter quartz tube furnace, which was evacuated to 2 mTorr, and subsequently heated to 400 °C under a 25 sccm flow of H_2 at 325 mTorr. After a 30 min soak, the temperature was ramped slowly to 1025 °C for 60 min to promote Cu grain growth (mean grain sizes exceeded 5 mm^2 as determined by optical microscopy). An initial low-density nucleation and slow growth phase was performed at 1025 °C for 90 min with a mixture of CH_4 and H_2 at a total pressure of 100 mTorr and flows of <0.5 and 2 sccm, respectively. Full coverage was achieved by dropping the temperature to 1010 °C for 10 min while increasing the total pressure and methane flow to 900 mTorr and 30 sccm, respectively.

Gold strips (2×10 mm^2) were evaporated onto the graphene that grew on the polished side of the foil followed by a thick 3 μm film of PMMA (MicroChem, 11% in Anisole) spun-cast at 500 rpm for 30 s and baked at 90 °C for 2 h. The uncoated graphene grown on the unpolished backside of the Cu was etched in an O_2 plasma and the Cu was etched away in a 2 h ammonium persulfate solution (Transene, APS-100) bath. The resulting PMMA/Au/graphene sandwich was trimmed, leaving some unprotected graphene surrounding the Au-protected regions, and rinsed in DI water and isopropyl alcohol.

An 8 nm layer of BCB (Dow Chemical Co., Cyclotene 3022-35), diluted in trimethylbenzene was spun onto p^+/SiO_2 wafers (Silicon Quest International, <0.005 Ohm-cm, 200 nm oxide). The BCB layer was subsequently hard baked at 300 °C for 1 h on a hot plate in an Ar glovebox, to ensure complete cross-linking after which it becomes impervious to solvents. The PMMA/Au/graphene sandwich was transferred to the BCB side of the wafer by clamping for 3 h at 80 °C. The PMMA and excess graphene were removed by an O_2-plasma ash for 1 h and the gold was etched in an iodide solution (Transene, Au TFA Etchant). Au source contacts (40 nm) were evaporated directly onto the edge of the graphene electrode. Deposition and transfer of the dilute nanotube network is described elsewhere.[33] All samples were baked on a hot plate in the glovebox at 300 °C for 1 h to dedope the graphene and nanotube films. DNTT was used as received from Nippon Kayaku Co., Ltd. It was thermally evaporated from an effusion cell at 210 °C at a growth rate of 4 Å/s in a pressure of 5.0×10^{-7} Torr to a thickness of 500 nm. Au drain electrodes (30 nm) were deposited through a TEM grid shadow mask defining dozens of individual, hexagonally shaped pixels with a surface area of 0.035 mm^2.

Current density *versus* voltage (*J*−*V*) output and transfer curves were measured with a Keithley model 2612A source meter controlled by a program written in LabVIEW.

Raman spectra were acquired with a Horiba Jobin-Yvon LabRAM Aramis system using 532 nm excitation, ND-1 filter, 600 line diffraction grating, 6 s integration time, and 2× averaging. Scatterplot data was accumulated from 10×10 arrays with 50 μm spacing in both the *x* and *y* plane. SEM images were taken using a JEOL 5700 SEM and analyzed using ImageJ software to acquire hole statistics yielding their mean size and areal densities (details in Supporting Information).

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: AFM images of the copper foils used as the graphene growth substrates before and after the CMP; maps of the Raman D band intensity and the D/G band intensity ratios for films transferred with and without the Au interlayer; an example SEM image of graphene with etched holes, the ImageJ software mask associated with this image from which a hole diameter histogram was obtained and hole diameter histograms from which areal hole densities were derived. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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