DOI: 10.1002/adma.200800601

Carbon-Nanotube-Enabled Vertical Field Effect and Light-Emitting Transistors**

By *Bo Liu, Mitchell A. McCarthy, Youngki Yoon, Do Young Kim, Zhuangchun Wu, Franky So, Paul H. Holloway, John R. Reynolds, Jing Guo,* and *Andrew G. Rinzler**

By experiment and supporting theory we demonstrate the facile modulation of the electronic contact-barrier across the junction between single wall carbon nanotubes (SWNTs) and two distinct organic semiconductors demonstrating a new realm of application for carbon nanotubes. We exploit this ability to enable two devices: a vertical field-effect transistor and a vertical light-emitting transistor. The vertical architecture, which is readily facilitated by the specific properties of the nanotubes, allows the use of low mobility semiconductors that would otherwise be considered unsuitable for field effect transistors, thereby expanding the range of potential active materials. For the light-emitting transistor the gate control should permit new pixel drive schemes and affords the potential for increased device lifetimes.

Thin-film transistors (TFTs) provide the drive circuitry for present and emerging active matrix displays including liquid-crystal and organic-light-emitting display technologies. The dominant active semiconductor in these devices is amorphous silicon, however the promise of inexpensive, solution-based processing techniques, inkjet patterning and construction on flexible plastic substrates has focused much research over the past 20 years on organic semiconductors as replacements. There now exists a broad range of small-molecule organic and polymeric compounds that have demonstrated transconductance. Unfortunately, the electronic mobilities of these compounds, which were initially about 5–6 orders of magnitude too low to be commercially useful, remain about an order of magnitude too low. Such low mobility can be compensated for by bringing the source and drain electrodes closer together reducing the semiconductor channel length (C_L in Fig. 1a), but that greatly raises the cost of patterning the devices, removing much of the motivation.

In 2004 Yang and coworkers demonstrated a new TFT architecture that they suggested could circumvent the mobility limitations of present organic semiconductors.[1] Their devices, however, relied on an ultrathin (<20 nm) aluminum source electrode that required careful partial oxidation. While the optimized device exhibited ~6 orders of magnitude current modulation, the low work-function aluminum source electrode required an n-type active channel restricting that device to the use of C_{60} as the channel material. Recently, the use of the more conventional organic semiconductor pentacene was demonstrated. However, this required the additional complication of a 7 nm vanadium oxide layer atop the partially oxidized aluminum source electrode.[2] Most recently they found that this architecture affords important new opportunities in how organic light-emitting diodes (the likely successor to liquid crystal displays) are electronically driven.[3] This is impressive work, but the requisite partly oxidized, ultrathin aluminum source electrode would be difficult to produce commercially, constrain the choices for the organic active layers, and be susceptible to electromigration, thus limiting device lifetimes. Working independently, using single-wall carbon nanotubes as the source electrodes, we have arrived at a similar departure from the conventional TFT architecture and also used them to develop a gate-controlled light-emitting diode. Here we describe the devices, highlighting the important advantages presented by using carbon nanotubes.We additionally communicate some previously unrecognized, relevant features in the physics of the nanotubes.

A TFT is a field effect transistor (FET) in which a gate field induces carriers in the active layer, permitting current to flow between the source and drain electrodes. Figure 1a and b compare, in schematic form, a conventional TFT and the new architecture. In contrast to the conventional TFT in which the source, active layer, and drain are co-planar with respect to the dielectric and gate, the new architecture stacks the source, active layer and drain vertically relative to the gate, hence the designation as a vertical field-effect transistor (VFET). For the VFET architecture a continuous metal source electrode would

[*] Prof. A. G. Rinzler, B. Liu, Z.-C. Wu
Department of Physics
University of Florida
P.O. Box 118440, Gainesville, FL 32611-8440 (USA)
E-mail: rinzler@phys.ufl.edu
M. A. McCarthy, D. Y. Kim, Prof. F. So, Prof. P. H. Holloway
Department of Materials Science and Engineering
University of Florida
P.O. Box 116400, Gainesville, FL 32611-6400 (USA)
Y. Yoon, Prof. J. Guo
Department of Electrical and Computer Engineering
University of Florida
P.O. Box 116130, Gainesville, FL 32611-6130 (USA)
Prof. J. R. Reynolds
Department of Chemistry
University of Florida
P.O. Box 117200, Gainesville, FL 32611-7200 (USA)

[**] We thank Dr. Ryan Walczak for calling our attention to the work by Yang and coworkers and are grateful to Arrowhead Research Corporation and Nanoholdings LLC for funding support. Supporting Information is available online from Wiley InterScience or from the authors.

ADVANCED MATERIALS

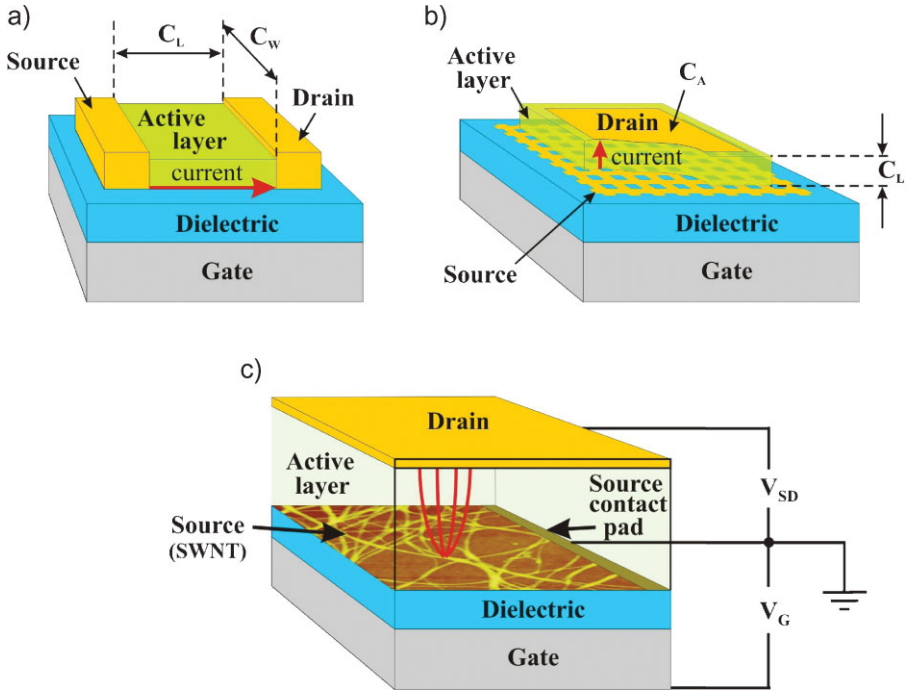

Figure 1. The standard TFT (a) and the VFET (b,c) architectures. An AFM image of our percolating nanotube network source electrode (scale ~0.5 μm × 1 μm) is shown in (c). Also shown is the wiring diagram for the device. A short channel length, C_L in the standard TFT requires tight patterning of the source and drain electrodes, an issue circumvented in the VFET. The current in the standard TFT (red arrows and lines indicate paths) scales with the channel width C_W, while in the VFET this scales with the overlap area between the source and drain electrodes, C_A.

completely screen the gate field from the active layer, hence a necessary requirement for its operation is that the source electrode be in some sense perforated, rendering it porous to the gate field. The source electrode shown as a regular grid in Figure 1b is meant to convey this idea but should not be taken literally. Yang's group achieved their gate-field-porous source electrode by the partial oxidation of a very thin aluminum film.[1] Our gate-field-porous source electrode is a network of single wall carbon nanotubes, in a dilute layer that is nevertheless well above the percolation threshold. Note that for the VFET the channel length C_L is simply the active layer film thickness, which can be made almost arbitrarily thin, without the need for high resolution electrode patterning.

Figure 2a and b show the transfer (I_{DS} vs. V_G) and output (I_{DS} vs. V_{DS}) curves for our devices using poly[(9,9-dioctyl-fluorenyl-2,7-diyl)-*alt-co*-(9-hexyl-3,6-carbazole)] (PF-9HK) as the active semiconductor layer and gold as the drain electrode. Also shown in Figure 2a is the transfer curve (output curve in Fig. 2c) for *N*,*N*′-di(1-naphthyl)-*N*,*N*′-diphenyl-1,1′-diphenyl-1,4′-diamine) (NPD) used as the active semiconductor layer. The gate voltage sweep modulates the current in both channel layers by two orders of magnitude. The large subthreshold slope is a consequence of the relatively thick SiO_2 gate dielectric used. Common practice in organic TFT research is the use of thinner gate dielectrics (to report better device characteristics). However, these generally leak at the typically high gate voltages needed and require a leakage current subtraction to yield accurate source-drain currents. In exploring a new device architecture we considered it prudent to avoid gate leakage by use of a thicker dielectric layer avoiding complications that could put the device function into question. The device characteristics can be anticipated to improve as the dielectric is made thinner. Note that in contrast to standard FETs where the on-current scales with the channel width (a linear dimension), current in the VFET scales with the overlap area between source and drain electrodes (a linear dimension squared). The on-current should also scale with the density of nanotubes in the source electrode (up to a limiting density at which the gate field begins to be screened by the nanotubes themselves).

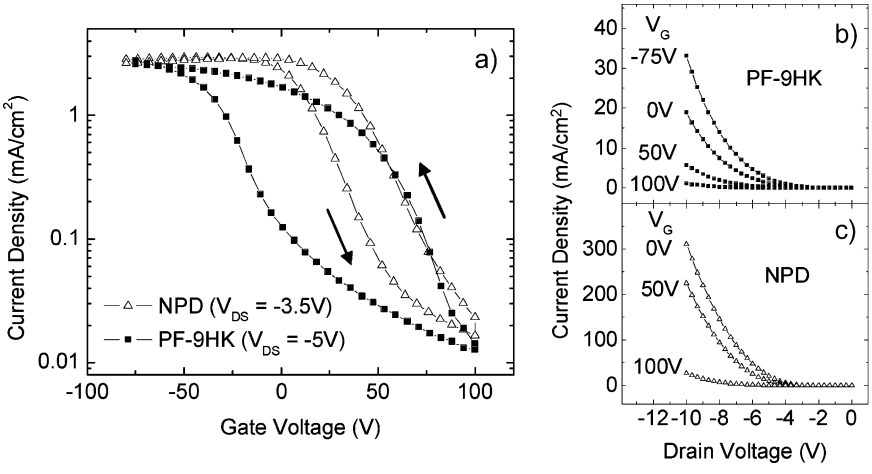

Figure 2. Transistor characteristics of the hole-only VFETs. a) Source-drain current as a function of the gate voltage for both material systems. PF-9HK devices display noticeably larger hysteresis than the NPD devices. Arrows indicate the gate voltage sweep direction. (b) Output curves for the PF-9HK VFET and (c) NPD VFET at the gate voltage specified adjacent to each curve.

Evident in the transfer curves in Figure 2a is a large hysteresis, likely caused by charge traps in the active layers employed. The hysteresis is substantially smaller for the NPD device over the PF-9HK based device, indicating that the hysteresis can be reduced by modification of the active layer.

In a standard organic TFT the Fermi levels of the source and drain electrodes are selected to be closely aligned with either the highest occupied molecular orbital (HOMO) or the lowest unoccupied molecular orbital (LUMO) of the active layer material, leading to a hole carrier (p-type) or an electron carrier (n-type) device, respectively. For some nominal source-drain voltage the gate field modulates the carrier density in a thin region at the active-layer/dielectric interface thus modulating the current that flows between the source and drain. Our experiments and theoretical modeling show that the principle mechanism by which the VFET operates is different. While modulation of the carrier density throughout the bulk of the active layer is indicated by simulation to be possible in the VFET geometry for very thin active layers, the resulting current modulation is a steep function of the active layer thickness. This arises because carriers generated nearest the gate electrode tend to screen the gate field from deeper regions of the active layer. For active layer thicknesses >100 nm such screening would result in only a small response of the source-drain current to the gate field. The large modulation observed for the >100 nm active layers used and only weak dependence of the gate-field lever arm on the active layer thickness (as observed in our experiments) strongly implicates a gate-induced modulation of the contact barrier between the nanotubes and the active layer. Since gated nanotube networks have demonstrated transconductance,[4] it might be thought that this phenomena is relevant here, but achieving appreciable current modulation across nanotube networks requires the nanotube surface density be very near percolation[5] such that the threshold percolation pathways bridge across semiconducting nanotubes (i.e., the metallic nanotubes, considered alone, must lie below the percolation threshold). Well above percolation in the metallic tubes (our range), with typically 1/3 metallic and 2/3 semiconducting nanotubes, the turn on of the semiconducting nanotubes can account for a factor of ~2/3 or ~0.67 of the modulation, not the factor of >100 observed. This indicates that the devices function as p-type, Schottky barrier FETs in which the current modulation is due to a gate-field-induced modulation of the contact barrier at the nanotube/active layer interface. Modeling of the injection barrier and the effect of gate field on it indeed shows this to be the case.

A two-dimensional Poisson equation was solved self-consistently with the equilibrium carrier statistics of the polymer channel and the nanotube contact for a structure as shown in the inset of Figure 3. In order to simplify the modeling and capture the essential physics, the following assumptions were made: (i) the nanotube network is sparse so that an individual nanotube is studied for electrostatics in each region, (ii) a 2D cross-section in a vertical plane perpendicular to a nanotube long axis is simulated, and (iii) the nanotube is an individual single-walled metallic tube. A semiconducting nanotube or a small bundle has a different density of states but does not change the qualitative results. Figure 3 shows the band bending at the nanotube/active layer interface as a function of the gate field, displaying the barrier modulation.

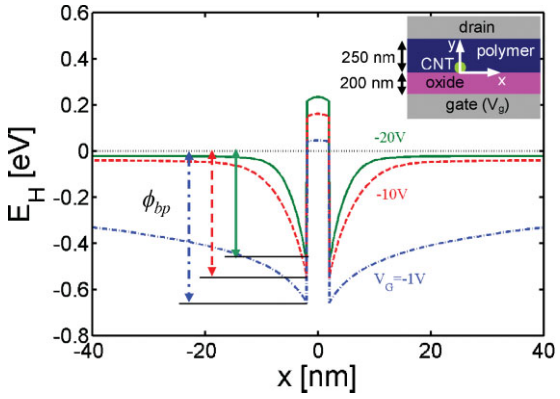

Figure 3. The HOMO versus the horizontal position x at different gate voltages, $V_G = -1$ V, -10 V, and -20 V taken at the vertical position $y = 1$ nm, where the interface between the gate oxide and the polymer channel is defined as $y = 0$. The equilibrium Fermi level in both the polymer channel and the nanotube contact is $E_F = 0$ (horizontal dotted line). Vertical arrows indicate the barrier height ϕ_{bp} at each voltage. The nanotube diameter is 5 nm with its center located at $x = 0$ and $y = 2.5$ nm. The inset shows the simulated structure and the coordinates. Inside the nanotube ($|x| < 2.5$ nm) the electron potential energy (the symmetric point of the p_z orbital bands, see Supporting Information) is plotted.

A new and important feature demonstrated here stems from the intrinsic low density of states (DOS) for the nanotubes. In contrast to metals, which possess a high DOS, the Fermi level of the low DOS nanotubes can undergo an appreciable shift in response to the gate field. Hence, in addition to the thinning of the contact barrier due to the gate-induced band bending, the barrier height (ϕ_{bp}) is also lowered. Literature descriptions of contact barrier modulation at metallic Schottky contacts are often mislabeled as barrier height modulation when what is really meant is barrier width modulation due to band bending. The high DOS of metals simply does not permit the Fermi level shift necessary for a change in the barrier height. The first report of a true barrier height modulation (of which we are aware) is the electrochemically induced barrier height modulation in an air-sensitive polymer/inorganic (poly(pyrrole)/n-indium phosphide) contact barrier, first demonstrated by Lonergan in 1997[6] (although even here, the polymer is not a true metallic system, as are the nanotubes). The nanotubes exhibit this characteristic, as an air stable material, permitting its ready exploitation.

The gate-induced band bending and barrier height modulation shown in Figure 3 are the result of the simulation at a distance of 1 nm from the gate dielectric surface. The degree to which these effects occur also depends on the distance from the gate. Self screening by the nanotubes reduces the gate lever arm in going from the bottom side of a nanotube, nearest the dielectric layer, to its top side. This implies that individual nanotubes are preferred over nanotube bundles since the top

ADVANCED MATERIALS

nanotubes in a bundle are screened from the gate field by underlying nanotubes and participate substantially less in the modulation. Our nanotube networks are formed by a filtration/transfer method[7] from pulsed laser vaporization grown nanotubes. All high yield nanotube synthesis methods produce bundles of varying diameter and while ultrasonication in surfactants provides a measure of bundle disassembly, excess ultrasonication can also damage and shorten nanotubes. AFM imaging and height analysis statistics shows our networks to be comprised of a bundle distribution ranging in diameters from 1 to 9 nm with a peak centered at ~5 nm (see on-line Supporting Information).

A requirement that constrains the useful active layer materials in such devices is that the HOMO lies within reach of the nanotube Fermi level for rationally applicable gate fields. If the active layer HOMO lies above the nanotube Fermi level the gate field must generate a barrier at the accumulation layer (anti-barrier) for holes, while if the active layer HOMO lies below the nanotube Fermi level the gate must reduce the pre-existing barrier. Bundled nanotubes in the network impose more severe constraints on the active layer materials that will yield useful transconductance. For active layers possessing a normally on (anti-barrier) band line-up, the top nanotubes in a bundle screened from the gate, can not switch their barriers off. Because those nanotubes permit current flow independent of the gate field, such normally on devices can not be turned off effectively, greatly reducing the on/off ratio. For active layers possessing a normally off band line-up, the current is switched on by the nanotubes near the bottom of the bundles. Although the top nanotubes in the bundles participate little in the switching, they do not degrade the on/off current ratio. These inferences are supported by the large on-off ratios observed for PF-9HK and NPD (HOMOs ~5.6 eV[8] and ~5.5 eV,[9] respectively, versus our acid purified p-doped SWNT, work function ~4.9 eV) in contrast with a poor on/off ratio observed with regio-regular poly(3-hexylthiophene) (HOMO ~5.0 eV[10,11]) used as active layer (data not shown).

Further distinction between the nanotubes and metallic contacts bears mention. Metals are susceptible to bond formation with active layers that possess a covalent character. Such covalent bonds are implicated in a frequently observed insensitivity of the barrier height formed to the work function difference between the metal and semiconductor (Fermi level pinning). Pristine nanotubes by virtue of their highly passivated, graphene-like surface do not readily form covalent bonds, leaving the barrier height predisposed to gate modulation. Defects on the sidewalls of real world nanotubes may modify this picture, however, a) measures can be taken to minimize or heal defects, and b) whether or not defects in a quasi-1D system can engender Fermi-level pinning is an interesting, open question that such devices can begin to address. Other advantages afforded by the nanotubes are that the strength with which carbon atoms are held within the nanotube sidewall lattice is such that nanotubes are impervious to electromigration,[12] a key lifetime-limiting mechanism in most metal-contact-based electronic and electro-optic devices. Finally, the quasi-1D geometry of a nanotube contact results in favorable junction electrostatics. The electric field at the surface of the nanotube is significantly enhanced due to its nanometer-scale radius. The barrier thickness is thus further reduced, facilitating carrier injection from the nanotube contact into the active channel.

PF-9HK, initially selected for its low lying HOMO, is also an electroluminescent polymer. This naturally led to the idea that simple modification of the top contact to an electron-injecting, small work-function metal could turn the formerly hole-only device into a gated, organic light-emitting diode (OLED), where electrons injected from the top contact and holes from the nanotubes recombine across the polymer bandgap to produce light. Such devices indeed work, allowing control of the emitted light intensity by the applied gate voltage suggesting the nomenclature: vertical organic light-emitting transistor (VOLET). To demonstrate the general applicability of the design, Figure 4 shows gated light emission in a different system: tris(8-hydroxyquinoline) aluminum (Alq_3) as the photoactive layer, NPD as the hole transport layer, and PF-9HK as the gated, hole-injecting layer. To permit light extraction, the gate electrode is ITO on a transparent substrate with a 160 nm atomic-layer-deposited aluminum-titanium oxide (ATO) gate dielectric on which the nanotube network lies. For devices in which the NPD layer directly contacted the nanotubes, for reasons yet to be determined, light was initially emitted but with a quickly decaying luminance (despite long-term stable operation of the hole only VFETs using NPD in

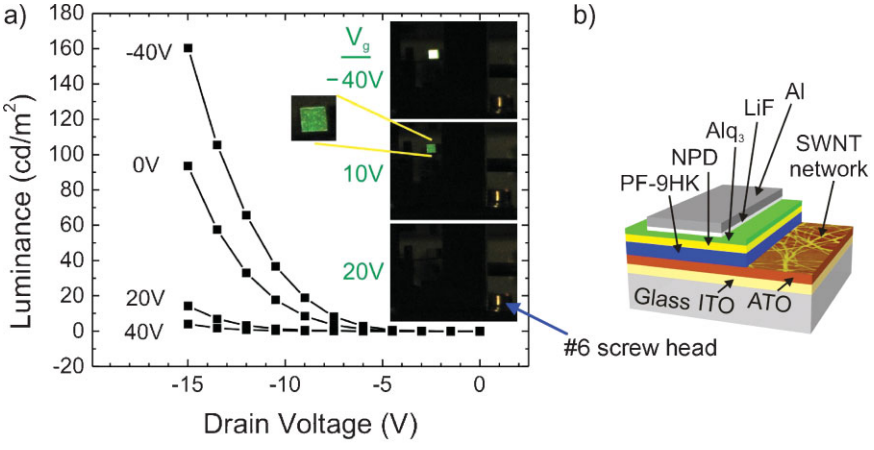

Figure 4. a) Luminance versus drain voltage at the indicated gate voltages for the VOLET stack illustrated in (b). The inset to (a) shows photographs of the light emitted by a 2 mm × 2 mm pixel for −7 V drain voltage at the gate voltages indicated in green, with a zoom on the pixel in the center image. A corresponding current density versus drain voltage plot at these gate voltages is provided in the on-line Supporting Information. Also in the Supporting Information are luminance and current density transfer curves.

direct contact with the nanotubes). This lifetime issue was resolved by addition of PF-9HK as the layer that contacts the nanotubes. A schematic of the device is shown in Figure 4b. In this hybrid polymer/small molecule device, the 200 nm PF-9HK layer was spun onto the nanotubes from toluene, and the NPD (100 nm), Alq_3 (50 nm), LiF (1 nm), and Al (100 nm) layers were all thermally evaporated. The inset of Figure 4a shows the gated light emission from the device at the gate voltages indicated (drain voltage −7 V in all cases). The pixel here is 2 mm × 2 mm (the cap head screw with a head diameter of 4.3 mm, which supports the device fixture, provides scale). Interestingly, given the thinness of the nanotube source layer, at a drain voltage of −30 V (where there is little gate modulation possible because the large source-drain voltage overcomes the major fraction of the barrier), the luminance is $540\,cd \cdot m^{-2}$, at a current density of $17.3\,mA \cdot cm^{-2}$, for a quite reasonable efficiency of $3.1\,cd \cdot A^{-1}$ (comparable to typical ITO anode, NPD/Alq_3-based devices). It is worth noting that the device shown is among the first such devices constructed with substantial room for optimization. Bright spots in the pixel zoom are likely caused by particulates that underlie the nanotube network resulting in a local thinning of the source-drain channel length. This is supported by the principal failure mode in the devices of direct electrical shorts between the source-drain electrodes as we thin the electroactive layers (for present fabrication controls). This issue also limited the performance of the VFETs and highlights the need for ultrahigh-purity nanotube material and cleanliness of the environment in the network fabrication. However, it also indicates that there are improvements to be obtained from thinning the electroactive layers.

It was not until these efforts were nearing completion that we were pointed to the work by Yang and coworkers on their VFET and VOLET design.[1–3] To further contrast our respective source electrodes, electrical percolation in nanotube networks is readily attained over a large range of nanotube densities, while permitting open regions between the high aspect ratio nanotubes for gate field penetration. The same cannot be said for quasi-spherical metallic grains, for which obtaining simultaneous electrical percolation and gate field porosity must necessarily present a delicate balance. Carbon nanotubes provide a natural path forward for the development of these new device architectures. Opportunities should abound.

Received: March 3, 2008
Revised: April 23, 2008
Published online: August 27, 2008

[1] L. Ma, Y. Yang, *Appl. Phys. Lett.* **2004**, *85*, 5084.
[2] S.-H. Li, Z. Xu, L. Ma, C.-W. Chu, Y. Yang, *Appl. Phys. Lett.* **2007**, *91*, 083507.
[3] Z. Xu, S.-H. Li, L. Ma, G. Li, Y. Yang, *Appl. Phys. Lett.* **2007**, *91*, 092911.
[4] E. S. Snow, J. P. Novak, P. M. Campbell, D. Park, *Appl. Phys. Lett.* **2003**, *82*, 2145.
[5] H. E. Unalan, G. Fanchini, A. Kanwal, A. Du Pasquier, M. Chhowalla, *Nano Lett.* **2006**, *6*, 677.
[6] M. C. Lonergan, *Science* **1997**, *278*, 2103.
[7] Z. Wu, Z. Chen, X. Du, J. M. Logan, J. Sippel, M. Nikolou, K. Kamaras, J. R. Reynolds, D. B. Tanner, A. F. Hebard, A. G. Rinzler, *Science* **2004**, *305*, 1273.
[8] J.-H. Jou, M.-C. Sun, H.-H. Chou, C.-H. Li, *Appl. Phys. Lett.* **2006**, *88*, 141101.
[9] E. W. Forsythe, V. E. Choong, T. Q. Le, Y. Gao, *J. Vac. Sci. Technol. A* **1999**, *17*, 3429.
[10] M. Al-Ibrahim, H. K. Roth, M. Schroedner, A. Konkin, U. Zhokhavets, G. Gobsch, P. Scharff, S. Sensfuss, *Org. Electron.* **2005**, *6*, 65.
[11] K. Asadi, F. Gholamrezaie, E. C. P. Smits, P. W. M. Blom, B. de Boer, *J. Mater. Chem.* **2007**, *17*, 1947.
[12] K. Lee, Z. Wu, Z. Chen, F. Ren, S. J. Pearton, A. G. Rinzler, *Nano Lett.* **2004**, *4*, 911.