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High Current, Low Voltage Carbon Nanotube Enabled Vertical Organic Field Effect Transistors

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ABSTRACT State-of-the-art performance is demonstrated from a carbon nanotube enabled vertical field effect transistor using an organic channel material. The device exhibits an on/off current ratio $>10^5$ for a gate voltage range of 4 V with a current density output exceeding 50 mA/cm^2. The architecture enables submicrometer channel lengths while avoiding high-resolution patterning. The ability to drive high currents and inexpensive fabrication may provide the solution for the so-called OLED backplane problem.

KEYWORDS Vertical field effect transistor, carbon nanotube, low voltage, organic transistor

In contrast to the transistors that drive the pixels of liquid crystal displays (LCDs), the transistors that drive the pixels in active matrix OLED (AMOLED) displays must source high currents. Organic thin film transistors (TFTs) that operate with high output currents at low voltages have accordingly been a major research objective in recent years. Within the constraints of avoiding high-resolution patterning (to keep costs down) and the limited carrier mobility of organic materials, these two requirements are difficult to achieve simultaneously. The absence of an inexpensive solution for driving AMOLEDs has come to be called the OLED backplane problem. Besides ongoing efforts in the improvement of the charge transport properties of organic semiconductors, recent efforts have focused on reduction of the dielectric thickness and/or increasing the dielectric constant (k) of the gate insulator thereby increasing the gate capacitance. Progress has been significant with groups exploiting gate capacitances ranging from 44 to greater than 1100 nF/cm^2. TFTs employing a variety of active layers including pentacene,[1−8] a side-chain fluorinated fulleropyrrolidine (F17DOPF),[9] and phenyl-C61-butyric acid methyl ester (PCBM)[10] have been demonstrated, exhibiting on/off ratios of 10^4 to 10^6 at operating voltages less than 5 V with output currents ranging from 0.2 to 14 μA/mm of channel width. Recently Klauk and co-workers, combining a gate capacitance of 800 nF/cm^2 with a recently developed air-stable organic molecule (more below) demonstrated TFTs exhibiting state of the art performance: on/off ratios around 10^6, operating voltages less than 3 V, and output currents of 17 μA per millimeter of channel width.[11] Despite these advances, such output currents remain more than 2 orders of magnitude lower than those of polycrystalline Si TFTs operating at less than 5 V.[12] Competitiveness with poly-Si is perhaps too much to expect of organic materials; however there may be other ways to circumvent the comparatively low mobilities of the organics.

An architectural means to boost TFT currents is a transistor with a vertically oriented channel where the channel length is determined by the thickness of the semiconductor thin film layer. This allows for submicrometer channel lengths without the need for high-resolution patterning. Yang and co-workers demonstrated a vertical organic field effect transistor (VFET) based on a thin, partly oxidized Al source electrode using P3HT as the active layer and a LiF supercapacitor as the dielectric (with a gate capacitance >1 μF/cm^2). They achieved ~17 mA/cm^2 output current at less than 5 V operating voltages with on/off ratios on the scale of 10^3. However such devices require a humid environment for the LiF supercapacitor material to function.[13] Others have also demonstrated VFETs of alternative[14,15] and similar[16] designs, but these did not exhibit low voltage operation.

Recently we demonstrated a carbon nanotube enabled VFET (CN-VFET). In this device the nanotubes are spread as a thin, percolating, source electrode layer across the gate dielectric; the nanotube layer is covered by the organic channel layer, which is in-turn covered by the top drain electrode (Figure 1). Current modulation in our device relies on the gate field modulation of a Schottky barrier that develops between the nanotubes and the organic channel material. Because of bundled nanotubes in the source layer, p-channel operation requires organic materials that form a barrier for hole injection greater than approximately 0.4 eV (e.g., for a nanotube workfunction of −4.9 eV the HOMO level of the organic channel should be −5.3 eV or deeper).[17] Our initial demonstration of this architecture used organic channel layers having carrier mobilities far lower than typical organic TFT materials and a gate dielectric consisting of a

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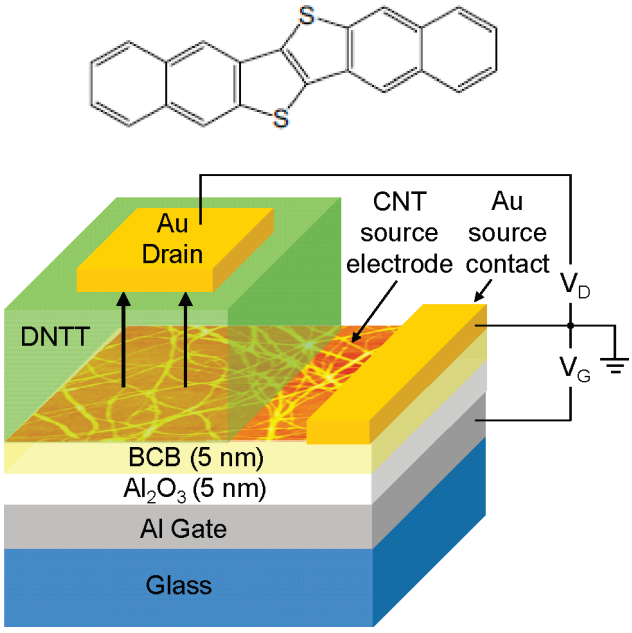

FIGURE 1. Schematic of the CN-VFET. The nanotube source electrode is depicted in the drawing by an AFM image with a scan size of ~1 μm × 1 μm. Also shown is the wiring diagram for the device. When the drain voltage is negative, holes are injected from the nanotube source electrode (held at ground) into the semiconductor layer and travel in the vertical direction (arrows) to be carried out by the drain. Shown on the top is the molecular structure of DNTT.

200 nm thick thermal oxide, possessing a capacitance of only 17 nF/cm^2. Nevertheless, the devices gave output currents of 3 mA/cm^2 at a drain voltage (V_D) of only 5 V. Because of the low capacitance of the thick dielectric layer, however, the devices required a gate voltage (V_G) of ±50 V for an on/off ratio of only 10^2.[17] Here we correct these deficiencies demonstrating a CN-VFET employing a high carrier mobility organic channel layer fabricated on a thin dielectric with a capacitance of 354 nF/cm^2. These modifications yield devices that meet or exceed state-of-the-art performance.

Yamamoto and Takimiya recently reported their synthesis and application of an air-stable small molecule with a high hole mobility: dinaphtho-[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]-thiophene (DNTT). In conventional TFT devices on Si/SiO_2 substrates with an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM), mobilities of 2.9 cm^2/(V s) were reported.[18] The highest occupied molecular orbital (HOMO) level of DNTT is at −5.4 eV. Compared to pentacene (HOMO level −5.0 eV), the deeper HOMO of DNTT renders it air stable. Shown in Figure 1 is the molecular structure of DNTT. The air stability of DNTT vs pentacene in TFT devices has been investigated by Klauk and co-workers. DNTT TFT devices retained 50% of their initial performance after 8 months in air whereas pentacene devices degraded by more than an order of magnitude after only 3 months.[11] This material combined with the 800 nF/cm^2 capacitance of a sub-6-nm bilayer dielectric of aluminum oxide and a SAM yielded the record performance mentioned above.[11]

The current in conventional lateral channel TFTs scales linearly with the length of the electrodes (the channel width). While the current in VFETs scales with the channel area, i.e., the area of the organic semiconductor sandwiched between the planar electrodes. To provide a figure of merit (FOM) that allows a direct comparison of the two types of devices, we convert the linear current density of a TFT into an effective areal current density (J_{Eff}). This is rationally done by assuming an interdigitated source−drain electrode pattern wherein the width of each source and drain finger is taken to be equal to the channel length of the TFT, thus preserving the resolution of the minimum feature size used for the channel. This interdigitated finger arrangement optimizes the areal usage for the lateral channel devices because every finger provides an electrode for the channel on each of its two sides (details for determination of J_{Eff} for the lateral channel TFTs are provided in the Supporting Information). The area occupied by the transistors is especially important in AMOLEDs where the drive transistor occupies pixel real estate and therefore reduces the organic light emitting diode (OLED) pixel aperture ratio (the fractional pixel area occupied by the OLED). Given that maximum on-current for minimum device area is desired, such on-current/device area provides an important FOM beyond the comparison with VFETs. With this FOM, the 17 μA/mm output current of the 30 μm channel length TFTs by Klauk and co-workers translates to a J_{Eff} of 28 mA/cm^2,[11] surpassing the 17 mA/cm^2 of the VFET by Yang and co-workers.[13]

Our device schematic is shown in Figure 1. The gate electrode was 60 nm of aluminum thermally evaporated onto glass substrates. An aluminum oxide dielectric layer was formed on the aluminum gate by O_2 plasma oxidation in a barrel asher, similar to that described in ref 19 but using longer times in the oxygen plasma to maximize the oxide thickness and thereby minimize leakage current. A thin hydrophobizing layer of a low-k dielectric: benzocyclobutene (BCB) was diluted in trimethylbenzene and spin coated to a thickness of ~5 nm.[20] The BCB layer was subsequently hard baked at 250 °C for 1 h on a hot plate in an Ar glovebox where it cross-links and becomes impervious to solvents. Contact to the CNT source layer was made by predeposited Cr/Au (8/40 nm thick, respectively) source contacts. The dilute nanotube source layer was fabricated as described previously.[21] Following nanotube layer deposition, the substrates were loaded into a dual Ar glovebox that contains separate organics and metals vacuum thermal evaporation systems permitting deposition of organic channel layers and metal contacts without exposure to ambient air. The substrates were baked on a hot plate in the glovebox at 225 °C for 1 h, prior to deposition of DNTT (details on the effect of the bake are in the Supporting Information). DNTT was used as received from Nippon Kayaku Co., Ltd. It was thermally evaporated from an effusion cell at ~210 °C at a growth rate of ~2.1 Å/s in a pressure of ~5.0 × 10^{-7} Torr to a thickness of 480 nm. Substrates were subsequently transferred to the

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metals evaporator, where 30 nm of Au was deposited as the drain electrode. The Au deposition was through a TEM grid shadow mask defining dozens of individual, hexagonally shaped pixels with the size for each hexagon of 200 μm between parallel sides (0.035 mm^2), completing the device construction. Current density vs voltage ($J-V$) output and transfer curves were measured with a Keithley model 2612A sourcemeter controlled by a program written in LabVIEW. To determine the quality and capacitance of our gate dielectric layers, metal−insulator−metal (MIM) capacitors were fabricated in a similar fashion except that the Au top contact was placed either directly onto the Al_2O_3 dielectric layer or onto the BCB hydrophobizing layer. Capacitance vs frequency curves were measured with an HP 4284A Precision LCR meter at a voltage amplitude of 100 mV.

Schematics of the test MIM capacitors are shown in parts A and B of Figure 2. The capacitance showed little dependence on frequency (Figure 2C) as is expected for the dielectrics used here. Adding an approximately 5 nm thick layer of BCB (as measured by AFM) to the Al_2O_3 reduced the capacitance (C) from 1710 to 354 nF/cm^2 but improved the reliability sufficiently to warrant its use. The thickness (d) of the Al_2O_3 was estimated from the capacitance of the bare Al_2O_3 device using $d = k\varepsilon_0/C$ assuming $k = 9$[22] and was found to be ∼4.8 nm. Figure 2D shows the typical leakage current density for an Al_2O_3 and an Al_2O_3 + BCB MIM device. Devices tended to breakdown irreversibly once the leakage currents exceeded (3−10) × 10^{-6} A/cm^2 so a gate leakage current of 2 × 10^{-6} A/cm^2 was selected as the upper limit for this gate dielectric in CN-VFET testing. This corresponded to keeping the electric fields below 2 MV/cm, placing an upper limit of ±2 V on the gate voltage.

Figure 3A shows the transfer curves for a DNTT-based CN-VFET on the Al_2O_3/BCB dielectric at the drain voltages indicated. For the total gate voltage range of 4 V the device exhibits >10^5 on/off ratio (−0.1 and −1.0 V drain voltage curves) or >10^4 on/off ratio (−3 V drain voltage curve) with the latter attaining a fully on-current density of 110 mA/cm^2. The output characteristics of the device are shown in Figure 3B for gate voltages ranging from +2 to −2 V in −0.5 V steps. Figure 3C plots the on/off ratio (for $V_G = -2$ V on, divided by $V_G = +2$ V off) as a function of the on-current density as V_D was swept from 0 to −3 V. The on/off ratio of the device remains >10^5 to 50 mA/cm^2 and is still above 10^4 to beyond 110 mA/cm^2. If this CN-VFET were to drive an OLED, of comparable size, with a luminance efficiency of 4 cd/A, at a drain current density (J_{Drain}) of 25 mA/cm^2, the luminance of the OLED would be 1000 cd/m^2, which is 4 to 5 times brighter than a typical computer screen.

What appears to be saturation in the two most on output curves ($V_G = -1.5$ V and $V_G = -2$ V) of Figure 3B is distinct from the typical TFT saturation understood from the gradual channel approximation.[23] Its origin is rather explained by a voltage drop across the thin, resistive nanotube source electrode (10−15 kΩ/sq sheet resistance) in the region between the pixel under test and the Au contact to the nanotubes, which was ∼2 mm in these initial test devices. In the on-state the current is limited by this resistance. With the Au source contact held at ground this resistance causes the nanotube source (in the region of the active pixel) to drift away from ground, reducing the gate voltage it sees, resulting in the apparent saturation. This series resistance is responsible for the roll-off seen in the on/off ratio at high current densities (Figure 3C) and can be mitigated by minimizing the distance between the CN-VFET pixel and its source contact.

To obtain an initial sense of device-to-device uniformity, 20 devices were characterized. Of these 20 devices, 10 shared one nanotube source electrode (CNT 1) and the other 10 shared a second, distinct, nanotube source

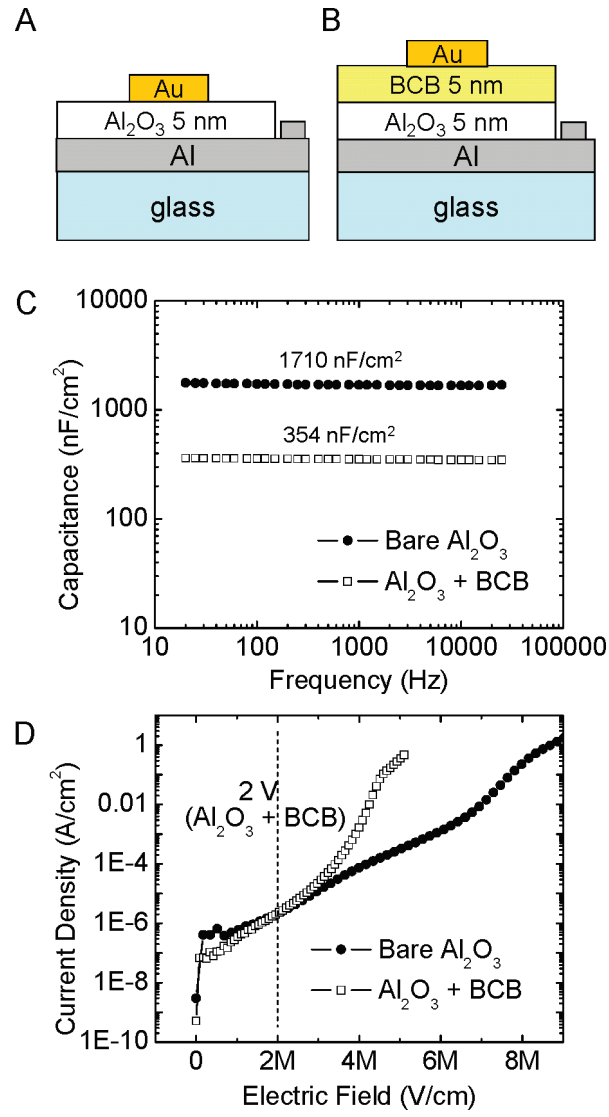

FIGURE 2. The MIM schematics for (A) the bare Al_2O_3 device and (B) the Al_2O_3 + BCB device. (C) Capacitance vs frequency plot for both MIM devices. (D) The leakage current density vs applied electric field. The leakage current density remains low below ∼2 MV/cm applied field.

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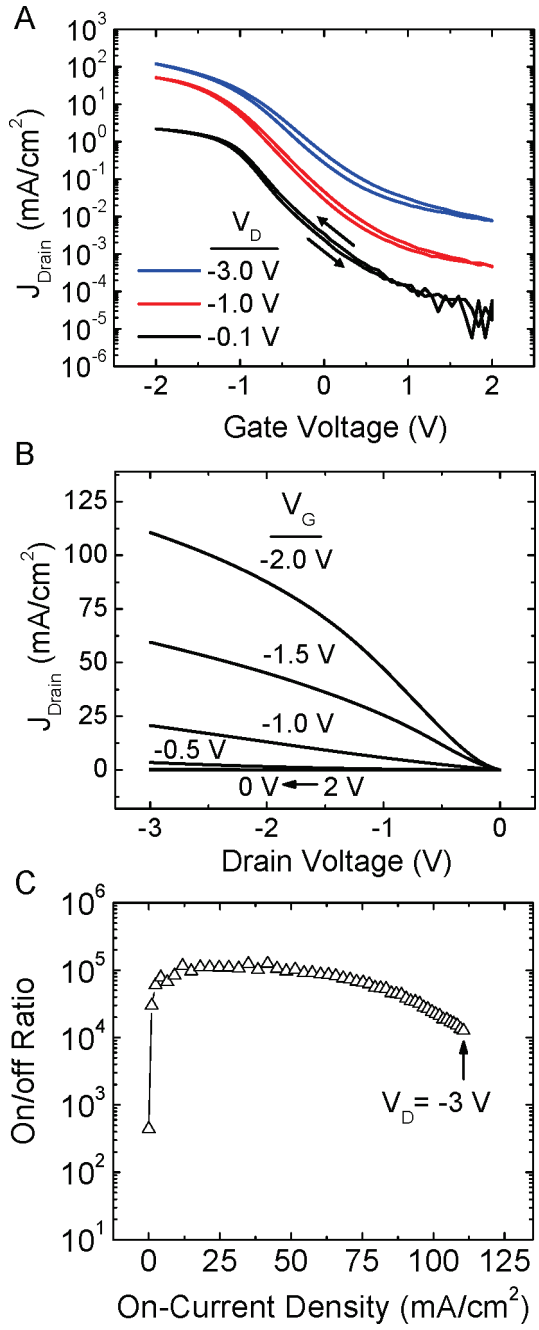

FIGURE 3. (A) Transfer curves of the CN-VFET at the indicated drain voltages. The curves show little hysteresis over the small gate voltage range of 4 V. (B) Output curves from $V_G = +2$ to -2 V in -0.5 V steps. (C) On/off ratio as a function of the on-current density, which stays above 10^5 to 50 mA/cm^2.

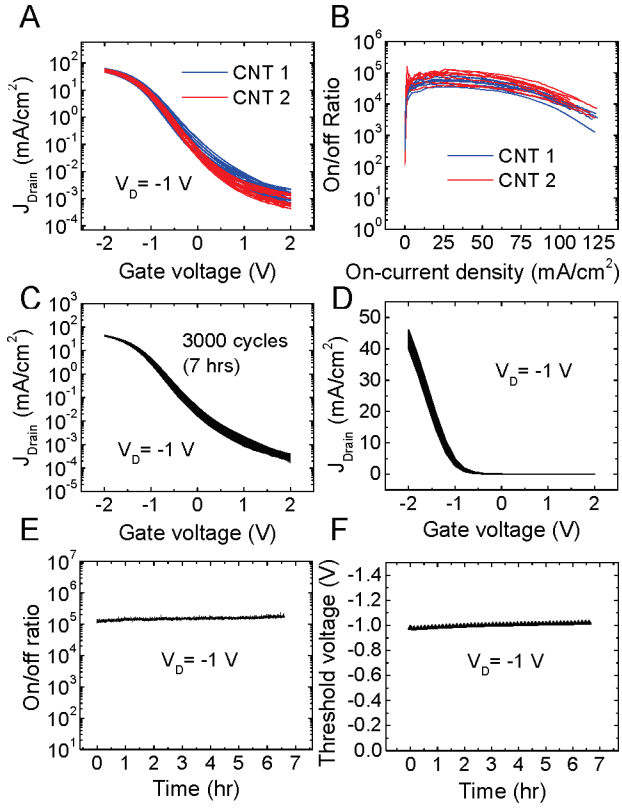

FIGURE 4. Uniformity (A and B) and stability (C–F) of the devices. (A) Transfer curves of 20 devices 10 on CNT 1 and 10 on CNT 2 source electrodes. (B) On/off ratio of the 20 devices. (C) Stability of one CN-VFET for 3000 transfer cycles over a period of 7 h at $V_D = -1$ V on a log–linear plot (highlighting changes in the off current density). (D) The same data on a linear–linear plot (highlighting changes in the on-current density and V_{Th}). (E) The on/off ratio from (C) is increasing with cycling. (F) The small drift in V_{Th} from (D), which appears to be saturating.

electrode (CNT 2). Optical microphotographs of the devices are shown in the Supporting Information. Figure 4A overlays the transfer curves for the 20 devices and Figure 4B shows their on/off current ratio versus the on-current density. The clear grouping of the data by the CNT electrodes suggests some variation in the nanotube source electrodes (perhaps in the nanotube density, but further work is needed to understand this). Statistics derived from these plots are shown in Table 1 (extraction of the threshold voltage is discussed below). The standard deviation for the maximum drain current density is 7% while that for the threshold voltage is 2%.

To investigate the effect of bias-stress on a CN-VFET, one device was cycled on and off, at a drain voltage of -1 V, 3000 times over a period of 7 h (1 cycle every 8 s). Measurements were performed in an argon glovebox. Parts C and D of Figure 4 show transfer curves for all 3000 scans (both scan directions) superimposed on a log–linear and a linear–linear scale, respectively. The on/off ratio increased slightly with cycle number during the 7 h scan (Figure 4E), starting at 1.2×10^5 and ending at 1.8×10^5. Plotting the transfer data on a linear–linear scale (Figure 4D) is useful for extracting the threshold voltage (V_{Th}) in order to detect bias-stress-induced shifts (Figure 4F) and for assessing device to device uniformity (Table 1). For a conventional TFT the threshold voltage is calculated from a linear fit on an $I_D^{1/2}$ vs V_G plot (based on the gradual channel approximation) and defined to be where the extracted regression line intersects the x axis.[23] Because the CN-VFET is a Schottky barrier

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TABLE 1. Statistics for the 20 Devices Measured for Uniformity in Parts A and B of Figure 4[a]

	max J_{Drain}[b] (mA/cm^2)		on/off ratio[c]		V_{Th} (V)		SS slope (mV/dec)	
	CNT 1	CNT 2	CNT 1	CNT 2	CNT 1	CNT 2	CNT 1	CNT 2
av	115	112	6×10^4	8×10^4	−0.93	−0.93	520	460
std dev	7	8	1×10^4	3×10^4	0.03	0.01	30	10

[a] Each value is calculated from 10 individual devices sharing either CNT 1 source or CNT 2 source electrodes. [b] At $V_D = -3.0$ V, and $V_G = -2.0$ V. [c] At 25 mA/cm^2 on-current density.

TABLE 2. Comparison of the CN-VFET to the Highest Performance, Low Patterning Resolution Devices Reported[a]

ref	device type	material	oper V(V)	I_{ON}/I_{OFF}	SS slope (mV/dec)	channel L (μm)	J_{eff} (mA/cm^2)	gate cap (nF/cm^2)
11	TFT	DNTT	3	10^6	100	30	28	800
1	TFT	pentacene	2	10^5	78	80	1.3	950
8	TFT	pentacene	5	10^5	317	70	1.1	76
6	TFT	pentacene	2	10^4	160	25	2.8	1100
13	VFET	P3HT	5	10^3	500[b]	?	17	1000
this work	VFET	DNTT	4	10^5	500	0.5	110	354

[a] Low patterning resolution is here defined as channel lengths >25 μm (for the TFTs). Other criteria for inclusion were p-type devices for air stability, on/off ratios (for the TFTs) >10^4, operating voltages <5 V, and effective current densities (J_{eff}) > 1 mA/cm^2. [b] Estimated from output data (transfer data not shown).

device,[17] the equations from the gradual channel approximation are not relevant. Instead, because the J_{Drain} of the CN-VFET follows a nearly linear dependence on V_G in the on-state, it is natural to extract V_{Th} from the linear J_{Drain} vs V_G plot (Figure 4D). During the cycling period, V_{Th} shifts from −0.98 to −1.02 V (Figure 4F).

Table 2 compares the performance of state-of-the-art, organic channel devices reported in the literature for which the criteria for inclusion were low-resolution patterning (channel lengths >25 μm for TFTs to preserve inexpensive manufacturing), p-type channel materials (for greater air stability), on/off ratios for the TFTs > 10^4, operating voltages <5 V, and effective current densities (J_{eff}) > 1 mA/cm^2. The CN-VFET achieves its low operating voltage despite the comparatively modest gate capacitance, which bodes well for device reliability. The output current density of the CN-VFET exceeds even the best of the other devices by a factor of 3.9. This excess current handling capacity is important for driving the high currents required by OLED pixels. Moreover, to achieve their highest effective current densities, the TFT devices required patterning that approached the smallest feature size for inclusion in the table (25 μm). The minimum patterned feature size of the CN-VFET in these studies was 200 μm (the drain electrode). These results are from the initial set of devices made with the Al_2O_3 gate dielectric and BCB, so we anticipate significant room for further optimization. Additional advantages of the nanotube source electrode include imperviousness to electromigration (a potential lifetime limiting mechanism with other source electrodes) and the transparency of the thin nanotube source layer (>98% transmittance), which lends itself to the construction of a light emitting transistor.[17] On the basis of these results we contend that the CN-VFET, requiring only materials available today, is in a promising position to solve the OLED backplane problem, accelerating the energy saving evolution from LCD to OLED display technology.

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Supporting Information Available. Additional data showing the effect of baking the nanotube network along with a detailed description of the J_{Eff} calculations for the TFTs appearing in Table 2 and optical microphotographs of the CN-VFET devices. This material is available free of charge via the Internet at http://pubs.acs.org.

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